3993 65376

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

Rev. 8/27/01 This is an experimental format – Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 4/25/02 Serial # 09/854,269 Priority Application Date ~~5/14/01~~ 9/18/97

Your Name M. Lewis Examiner # _____

AU 2829 Phone 305-3743 Room Plaza 3-3807

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Problems (See Paragraph 3, 4-8

Solution (" " 15 + 16

" Abstract

dielectric - polymeric materials

ex. polyimide

Claims 1-7

Staff Use Only

Searcher: Derrick Blakely

Searcher Phone: _____

Searcher Location: STIC-EIC2800, CP4-9C18

Date Searcher Picked Up: 5/2/02

Date Completed: 5/3/02

Searcher Prep/Rev Time: 70

Online Time: 215

Type of Search

Structure (#)_____

Bibliographic ✓

Litigation_____

Fulltext_____

Patent Family_____

Other_____

Vendors

STN ✓

Dialog_____

Questel/Orbit_____

Lexis-Nexis_____

WWW/Internet_____

Other_____

FILE 'REGISTRY' ENTERED
L1 46047 S PI/PCT
L2 1 S LEAD/CN
L3 1 S TIN/CN
L4 1 S COPPER/CN

FILE 'HCAPLUS' ENTERED
L5 247 SEA ABB=ON PLU=ON (SOLDERING OR SOLDERED OR SOLDER OR SOLDER OR BRAZ?)(4A)(COLUMN OR RANK OR ROW OR TIER OR MATRIX)
L6 163 S (SOLDERING OR SOLDERED OR SOLDER OR BRAZ?)(4A)(MASS##)
L7 1672911 S DIELECTRIC? OR OXIDE OR INSULAT?
L8 4959 S (CONTACT? OR BONDING OR CONNECT? OR JOIN?)(3A)(PAD OR PADS OR BUMP OR BUMPS)
L9 2207 S (COLUMN OR RANK OR ROW OR TIER OR MATRIX OR DETERMINANT OR COLUMNAR)(4A)(INCLUSION?)
L10 16 S (SOLDERING OR SOLDERED OR SOLDER? OR SOLDER OR BRAZ?)(4A)(COLUMNAR)

L11 2753 S L1(L)L7
L12 0 S L11 AND L5
L13 3 S L11 AND L8
L14 3 S L13 NOT L10
L15 0 S L11 AND L6
L16 0 S L11 AND L9
L17 29 S L11 AND TERMINAL
L18 12 S L6 AND ((L2 OR LEAD OR PB) AND (TIN OR SN OR L3) AND (CU OR COPPER OR L4))
L19 0 S L11 AND DISTAL
L20 1 S L5 AND DISTAL
L21 1 S L5 AND L6
L22 4 S L6 AND TERMINAL
L23 4 S L22 NOT (L13 OR L14 OR L17 OR L18 OR L21)
L24 6 S L11 AND PAD
L25 2 S L24 NOT (L13 OR L14 OR L17 OR L18 OR L21 OR L23)
L26 223842 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT?)) OR (MICRO)(W)(CIRCUIT? OR CHIP OR ELECTRONIC?) OR CHIP OR MICROCIRCUIT? OR DIE OR DICE OR LOGIC(W)CIRCUIT? OR WAFER OR MICROELECTRONIC? OR (CIRCUIT OR LOGIC)(2A)(CONFIGURATION)
L27 174 S L26 AND DISTAL
L28 12 S L27 AND TERMINAL
L29 12 S L28 NOT (L13 OR L14 OR L17 OR L18 OR L21 OR L23 OR L25)
L30 1 S L27 AND L5
L31 0 S L30 NOT L20
L32 0 S L27 AND L8

L33 1546670 S CONNECT? OR JOIN### OR COMBINE OR CONJOIN? OR CONJUGATE OR CONSOLIDATE OR COUPL? OR LINK### OR UNIF### OR UNITE OR YOKE
L34 46 S L27 AND L33
L35 12 S L34 AND (PACKAGE? OR BODY OR ENCAS? OR PROTECT? OR CASING OR CASE OR CAVITY OR ENCAPSULAT? OR CAPSUL? OR CASE OR CONTAIN? OR JACKET?)
L36 7 SEA ABB=ON PLU=ON L35 NOT (L13 OR L14 OR L17 OR L18 OR L21 OR L23 OR L25 OR L29)
L37 31 S L34 NOT (L13 OR L14 OR L17 OR L18 OR L21 OR L23 OR L25 OR L29 OR L36)
L38 0 S L37 AND (PAD OR BUMP)
L39 6 S L37 AND L7
L40 188 S L11 AND L26
L41 113 S L40 AND (PACKAGE? OR ENCAS? OR PROTECT? OR CASING OR CASE OR BODY OR CAVITY OR ENCAPSULAT? OR CAPSUL? OR CASE OR CONTAIN? OR JACKET?)
L42 13 S L41 AND L33
L43 11 S L42 NOT (L13 OR L14 OR L17 OR L18 OR L21 OR L23 OR L25 OR L29 OR L35 OR L36 OR L39)

L44 3 S L41 AND (PAD OR BUMPS)
L45 3 S L41 AND (PAD OR BUMP)
L46 1 S L45 NOT (L13 OR L14 OR L17 OR L18 OR L21 OR L23 OR L25 OR L29 OR L35 OR L36 OR L39 OR L43)

L47 1 S L41 AND (COLUMN OR COLUMNAR)
L48 1 S L40 AND (COLUMN OR COLUMNAR)

L10 ANSWER 3 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:247224 HCAPLUS
TI Semiconductor stacked device for implantable medical apparatus
IN Hubbard, Robert L.
PA Medtronic, Inc., USA
SO U.S., 22 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6051887	A	20000418	US 1998-143141	19980828
	US 6168973	B1	20010102	US 1999-292423	19990415
PRAI	US 1998-143141	A3	19980828		

AB A stacked semiconductor device is formed with a first mounting substrate, e.g., a single metal layer die tape, having a first semiconductor die attached thereto and a second mounting substrate, e.g., a double metal layer die tape having a second semiconductor die attached thereto. Substantially **columnar solder** connections, each formed from two solder balls are used to stack the first mounting substrate and the second mounting substrate such that the second semiconductor die is positioned between the mounting substrates. For example, identical memory dice may be stacked in this manner or different types of die such as a processor die and a memory die may be stacked in this manner for use in implantable medical apparatus.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L10 ANSWER 4 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:142046 HCAPLUS
DN 130:212741
TI Tip of iron and soldering iron having long service life and inhibiting tip corrosion
IN Kawashima, Tsutomu; Nishiki, Naoki; Maeda, Yukio
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11057996	A2	19990302	JP 1997-224967	19970821

AB The title tips comprise columnar carbon part as a heat supplier and metal

part. The carbon part has an edge for supplying heat, while an edge at the opposite side is joined with the metal part. The soldering irons have the above tips and heating app. and are suitable for electronic devices, plastic moldings, etc.

L10 ANSWER 5 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:505061 HCAPLUS
DN 129:210262
TI PTC current limiter and its production method.
IN Yoshizawa, Toshiyuki; Suzuki, Takaya; Kunihara, Kenji
PA Fuji Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10208908	A2	19980807	JP 1997-6039	19970117

AB In a PTC current limiter comprising a **columnar** V2O3 ceramic resistor, **soldered** electrodes on the ends of the resistor, and an oxidn.-prevention film of a low m.p. glass on the resistor, the diam. of the electrodes is wider than that of the resistor to prevent the formation of defects in the glass coating and to improve the reliability. A method for fabricating the limiter involves **soldering** a **columnar** V2O3 ceramic resistor using a soldering foil which has a thickness of 5-500 .mu.m and a diam. wider than that of the resistor.

L10 ANSWER 6 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:540619 HCAPLUS
DN 125:175021
TI Columnar potassium fluoroaluminate particles, their manufacture, and fluxes from them
IN Yamamoto, Koji; Mori, Kenzo
PA Tookemu Purodakutsu Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08157212	A2	19960618	JP 1994-329306	19941202

AB The process consists of treating Al(OH)3 with .ltoreq.20% HF at a mol ratio of Al:F 1:4-4.5 at 75-85.degree.; and neutralizing the fluoroaluminic acid soln. obtained with .ltoreq.15% KOH solns. to have slurry concn. .ltoreq.18%, and optionally pH at 1-9, to give K fluoroaluminate particles having av. diam. 12-20 .mu.m and aspect ratio 5-10. The K fluoroaluminate particles may have .gtoreq.50% 75 .mu.m-pore sieve permeability per 2 min. Fluxes contg. the particles for Al part brazing are also claimed.

L10 ANSWER 7 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:508827 HCAPLUS
DN 125:156246
TI Manufacture of bump electrode
IN Wakabayashi, Takeshi; Abe, Akihiko
PA Casio Computer Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08172096	A2	19960702	JP 1994-334322	19941216

AB The title method involves the following steps; forming a protective film on a substrate, forming a layer for formation of a metal underlayer on the protective film and a contact pad in a hole of the protective film, forming a 50-150-.mu.m plating resist layer, and forming a **solder columnar** bump electrode in the hole. A bump electrode with enough height was obtained.

L10 ANSWER 8 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:239999 HCAPLUS
DN 124:267627
TI Ball grid array package and its formation
IN Nakatani, Naoto
PA Nippon Avionics Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08051178	A2	19960220	JP 1994-202942	19940805

AB The ball grid array package consists of columnar lead pins on the I/O pads on the back side of a circuit board having semiconductor chips. The open ends of the lead pins are coated with a solder. The ball grid array package is formed by application of resist to the I/O pads, coating Cu on the pads to form **columnar** pins, application of a **solder** to the **columnar** pins, and melting the **solder** coating while holding the pins upside down to form a ball on the open end of a pin by gravity.

L10 ANSWER 9 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:39280 HCAPLUS
DN 124:151841
TI Brazing of steel and cast iron with copper filler metal
AU Steffens, H. -D.; Tuerpe, M.
CS Dortmund, Germany
SO DVS Ber. (1995), 166(Hart- und Hochtemperaturloeten und Diffusionsschweissen), 244-8
CODEN: DVSBA3; ISSN: 0418-9639
DT Journal
LA German
AB Brazing mild steel contg. different carbon contents with copper filler metal, the **braze** generally contains **columnar** phases. By this, the strength of brazed joints can be increased. The paper discusses the results of examns. that demonstrate the useful effect of columnar phases on the mech. properties of these joints.

L10 ANSWER 10 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:218850 HCAPLUS
DN 116:218850
TI The effect of columnar microstructure on the toughness of carbon steel braze joints

AU Ohmura, H.; Yoshida, T.; Kawashiri, K.
CS Dep. Met. Inorg. Mater., Nagoya Munic. Ind. Res. Inst., Japan
SO Weld. Res. (Miami) (1992), (March), 63-75 Published in: Weld. J. (Miami), 71(3)
CODEN: WERSA3; ISSN: 0096-7629
DT Journal
LA English
AB The effect on the Charpy U-notch impact toughness of a 0.17 C steel/1.04 C steel joint contg. a columnar Fe-(6-10)Cu-0.8C alloy phase was investigated. This phase comes from the dissoln. and deposit of the 1.04C base metal. The joint was brazed with AWS BCu-1 alloy at 498-873 K. The impact toughness of this joint was compared to that of other joints brazed with BAu-1, Bau-2, BAu-3, BAu-4, BNi-2, BAg8, and Cu-5Ni alloy fillers. When brazing with BCu-1 filler, the columnar structure exhibited a large effect on the impact toughness of the joint at 373-673 K. At 673 K, its impact toughness reached a max. value of 49 J. This value is .apprx.70% of that for joints brazed with BAu-2 and BAu-4, which have excellent toughness but no columnar microstructure. In the case of BAu-1, both base metals were joined by the columnar Fe-(5-6)Cu-(1-2)Au-0.8C alloy because of a lower Au content compared to that in BAu-2. Therefore the impact toughness of the joint was higher above 673 K than that made with BAu-2. As for the BNi-2 and BAg-8 **brazed** joints which have no **columnar** microstructure, the impact toughness was low throughout the whole temp. range. By using Cu-5Ni filler and BAu-3 instead of BCu-1 and BAu-1, compns. of the columnar phases became Fe-(12-16)Cu-(7-15)Ni-0.6C and Fe-7Cu-38Ni-(1-2)1Au-0.8C, resp. However, alloying the columnar phase with Ni did not increase the impact toughness of the brazed joints.

L10 ANSWER 11 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:65012 HCAPLUS
DN 116:65012
TI Composite braze for aluminum alloys
IN Kanai, Tomiyoshi
PA Showa Aluminium Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 03114690	A2	19910515	JP 1989-252910	19890928

AB The composite braze is manufd. by combining Al-Si-Zn alloy braze with Cu. The composite braze contains Si 8-15, Zn 6-15, and Cu 5-15%. Thus, Al-Si-Zn alloy braze was chill cast with a 4 mm-diam. Cu wire as the core to prep. a 20 mm-diam. **columnar** composite **braze**, and it was used for brazing of a AC4C block to a AA6063 Al alloy pipe. Sufficient fillet was formed in the brazed part.

L10 ANSWER 13 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1986:446923 HCAPLUS
DN 105:46923
TI High impact strength brazed joints
AU Ohmura, Hirohiko; Yoshida, Tohru
CS Nagoya Munic. Ind. Res. Inst., Nagoya, Japan
SO Yosetsu Gakkai Ronbunshu (1986), 4(2), 326-31
CODEN: YGRODU
DT Journal
LA Japanese
AB Methods to increase the impact strength of C steel brazed joints by utilizing dissoln. and deposition of the base metal were studied. Charpy U-notch impact strength of low-C steel (0.17%)/high-C steel (1.04%) joint brazed with a Cu filler was increased 2.9-27.2 J/cm2 at room temp. when both base metals were linked by a deposited columnar Fe alloy [94766-61-7] contg. 9-12 Cu and 1-2% C. When using a deposit-filler metal (high-C steel foil plated with Cu 10.mu. thick on both sides) for a similar low-C steel joint, impact strength of the joint increased to 89.4 J/cm2 because of linking both base metals with the columnar phase through the foil. Carburizing of 1 substrate to a depth of 0.2 mm enabled Cu brazing of a similar low-C steel joint. The resulting impact strength was 89.2 J/cm2 due to linking because the columnar phase deposited from the carburized low-C steel.

L10 ANSWER 14 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:82463 HCAPLUS
DN 102:82463
TI Deposition mechanism of columnar iron-copper-carbon alloy in copper brazing to dissimilar carbon steels
AU Ohmura, Hirohiko; Yoshida, Tohru
CS Nagoya Munic. Ind. Res. Inst., Nagoya, Japan
SO Yosetsu Gakkai Ronbunshu (1984), 2(4), 605-12
CODEN: YGRODU
DT Journal
LA Japanese
AB The C steels were brazed with Cu to study formation mechanism of columnar alloy structure. The Fe-(9-12) Cu-(1-2%) C [94766-61-7] columns were formed. When C steel dissolves into molten Cu, Fe and C atoms form the massive Fe carbides. In brazing of a low-C steel plate to a high-C steel plate, the columnar deposit is formed at the high-C plate side due to the massive Fe carbide from the low-C plate side in bonding with the C from the high-C side, to form the high-C masses with concns. exceeded the equil. level.

L14 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:851773 HCAPLUS
DN 135:379722
TI Wafer-scale assembly of chip-size packages
IN Heinen, Katherine G.; Edwards, Darvin R.; Jacobs, Elizabeth G.
PA USA
SO U.S. Pat. Appl. Publ., 17 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001044197	A1	20011122	US 1998-186973	19981105

AB A wafer-scale assembly app. for integrated circuits and a method for forming the wafer-scale assembly are disclosed. A semiconductor wafer including a plurality of circuits is provided with a plurality of metal **contact pads** as elec. entry and exit ports. A 1st wafer-scale patterned polymer film carrying solder balls for each of the **contact pads** on the wafer is positioned opposite the wafer and the film are aligned. The film is brought into contact with the wafer. Radiant energy in the near IR spectrum is applied to the backside of the wafer, heating the wafer uniformly and rapidly without moving the semiconductor wafer. Thermal energy is transferred through the wafer to the surface of the wafer and into the solder balls, which reflow onto the **contact pads**, while the thermal stretching of the polymer film is mech. compensated. The uniformity of the height of the liq. solder balls is controlled either by mech. stoppers or by the precision linear motion of motors. After cooling, the solder balls solidify and the 1st polymer film is removed. The process is repeated for assembling sequentially a wafer-scale patterned interposer overlying all of the solder balls and the wafer and contacting each solder ball with a soldered joint, and a 2nd wafer-scale patterned film carrying solder balls contacting the interposer. In each process, the wafer is heated uniformly and rapidly and without moving it, the alignment is maintained during heating by mech. compensating for the thermal stretching of the polymer film, and the uniformity of the height of the liq. solder balls is controlled by mech. stoppers or position closed-loop linear actuators. The 2nd film is removed after cooling. Other embodiments are also disclosed.

L14 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:94044 HCAPLUS
DN 134:140453
TI Design and fabrication of chip interconnect wiring structures with low dielectric constant insulators
IN Buchwalter, Leena P.; Callegari, Alessandro Cesare; Cohen, Stephan Alan; Graham, Teresita Ordonez; Hummel, John P.; Jahnes, Christopher V.; Purushothaman, Sampath; Saenger, Katherine Lynn; Shaw, Jane Margaret
PA International Business Machines Corp., USA
SO U.S., 18 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6184121	B1	20010206	US 1998-112919	19980709

PRAI US 1997-52174P P 19970710
AB A method to achieve a very low effective dielec. const. in high performance back end of the line chip interconnect wiring and the resulting multilayer structure are disclosed. The process involves fabricating the multilayer interconnect wiring structure by methods and materials currently known in the state of the art of semiconductor processing; removing the intralevel dielec. between the adjacent metal features by a suitable etching process; applying a thin passivation coating over the exposed etched structure; annealing the etched structure to remove plasma damage; laminating an insulating cover layer to the top surface of the passivated metal features; optionally depositing an insulating environmental barrier layer on top of the cover layer; etching vias in the environmental barrier layer, cover layer and the thin passivation layer for terminal **pad contacts**; and completing the device by fabricating terminal input/output pads. The method obviates issues such as processability and thermal stability assocd. with low dielec. const. materials by avoiding their use. Since air, which has the lowest dielec. const., is used as the intralevel dielec. the structure created by this method would possess a very low capacitance and hence fast propagation speeds. Such structure is ideally suitable for high d. interconnects required in high performance microelectronic device chips.
RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:713153 HCAPLUS
DN 121:313153
TI Studies on the high-temperature superconductor (HTS)/metal/polymer dielectric interconnect structure for packaging applications
AU Paik, Kyung W.; Mogro-Campero, Antonio
CS General Electric Corporate Research and Development, Schenectady, NY, 12301, USA
SO IEEE Trans. Compon., Packag., Manuf. Technol., Part B (1994), 17(3), 435-41
CODEN: IMTBE4; ISSN: 1070-9894
DT Journal
LA English
AB A HTS/metal/low dielec. const. polymer dielec. hybrid interconnect structure was fabricated using high d. interconnect (HDI) Cu/polyimide processing techniques. Non-degraded superconducting properties, Jc of over 1 MA cm-2 and Tc of 88 K, were obtained using optimum processing conditions. A 0.6 .mu.m-thick YBCO film was co-evapd. on LaAlO3 substrate, annealed, patterned, and Au **contact pads** were deposited. A Kapton polyimide film was laminated on HTS parts in an O environment. using a siloxane polyimide (SPI) base adhesive at 170-210.degree. or a polyester base adhesive at 150.degree. Vias were drilled on the polymer layer using a 351. nm Ar laser followed by subsequent via cleaning with O2 + CF4 plasma. To complete test parts Ti/Cu/Ti metalization and patterning with a laser adaptive lithog. were followed. The laminated polymer film on the HTS protected HTS film properties from heating and H2O exposure. The polyimide laminated HTS film maintains its supercond. up to 210.degree. of lamination temp. The hybrid structure also showed excellent reliability performances: 6% Jc decrease at 150.degree./65 h thermal bake, 12% Jc decrease after 100 thermal cycles from -96 to 150.degree., and maintain supercond. in H2O immersion up to >10 h. Tc of samples remained always the same 88 K. Coplanar HTS lines, microstrip HTS/metal lines, and HTS power strip line structures were demonstrated on a 2-in-diam. HTS wafer coupon.

L17 ANSWER 5 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:94044 HCAPLUS
DN 134:140453
TI Design and fabrication of chip interconnect wiring structures with low dielectric constant insulators
IN Buchwalter, Leena P.; Callegari, Alessandro Cesare; Cohen, Stephan Alan; Graham, Teresita Ordonez; Hummel, John P.; Jahnes, Christopher V.; Purushothaman, Sampath; Saenger, Katherine Lynn; Shaw, Jane Margaret
PA International Business Machines Corp., USA
SO U.S., 18 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6184121	B1	20010206	US 1998-112919	19980709
PRAI US 1997-52174P	P	19970710		

AB A method to achieve a very low effective dielec. const. in high performance back end of the line chip interconnect wiring and the resulting multilayer structure are disclosed. The process involves fabricating the multilayer interconnect wiring structure by methods and materials currently known in the state of the art of semiconductor processing; removing the intralevel dielec. between the adjacent metal features by a suitable etching process; applying a thin passivation coating over the exposed etched structure; annealing the etched structure to remove plasma damage; laminating an insulating cover layer to the top surface of the passivated metal features; optionally depositing an insulating environmental barrier layer on top of the cover layer; etching vias in the environmental barrier layer, cover layer and the thin passivation layer for **terminal** pad contacts; and completing the device by fabricating **terminal** input/output pads. The method obviates issues such as processability and thermal stability assocd. with low dielec. const. materials by avoiding their use. Since air, which has the lowest dielec. const., is used as the intralevel dielec. the structure created by this method would possess a very low capacitance and hence fast propagation speeds. Such structure is ideally suitable for high d. interconnects required in high performance microelectronic device chips.

RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 8 OF 29 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:129598 HCAPLUS
DN 126:165461
TI Multilayer thin film circuit board having electric insulator polymer film with controlled heat expansion coefficient
IN Takami, Seiichi
PA Kyocera Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08335778	A2	19961217	JP 1995-141633	19950608
JP 3164751	B2	20010508		

AB The circuit board consists of an elec. insulating support and alternatively laminated multilayer comprising org. polymer elec. insulator layers and metal layers as circuits, in which, the polymer contacted to the circuit layers attached to outer lead **terminals** shows thermal expansion coeff. 10 .times. 10-6/.degree.C-30 .times. 10-6/.degree.C. The polymer insulator layers are formed by thin film formation technique and the circuit layers are attached to the lead **terminals** through wax materials. The insulator layer may be a polyimide prepd. from pyromellitic dianhydride and 4,4'-diaminodiphenyl ether contg. 20% p-phenylenediamine-pyromellitic dianhydride copolymer.

=> D BIB AB 1-12

L18 ANSWER 1 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:273240 HCAPLUS
TI Power module. [Machine Translation].
IN Nonogaki, Ryozo; Sugimoto, Isao; Yokota, Hiroshi; Ibukiyama, Masahiro
PA Denki Kagaku Kogyo Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002110875	A2	20020412	JP 2000-304470	20001004

AB [Machine Translation of Descriptors]. It is superior in the heat dissipation, under truth using receiving the repetition of the temp. stress which repeatedly is worn, it offers the power module which maintains high reliability, cheaply. The surface **Cu** or **Cu** alloy or on the heat sink which consists of the Al or Al alloy, through the brazing filler metal, the elec. part through the solder with respect to the circuit where it possesses the circuit which consists of Al on the surface of the ceramic baseplate and in order the ceramic circuit baseplate which possesses the metallic plate on back, for the aforementioned metallic plate to touch to the brazing filler metal, connecting, becomes, furthermore consists of the description above Al connecting, being the power module which becomes, the aforementioned **solder** 45 **mass** % or more 85 mass % the power module which features that it is the **Sn-Pb** solder which contains **Pb** below.

L18 ANSWER 2 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:548148 HCAPLUS
DN 135:265127
TI A study on the fluxless soldering of Si-wafer/glass substrate using **Sn**-3.5 mass% Ag and **Sn**-37 **mass% Pb** **solder**
AU Park, Chang-Bae; Hong, Soon-Min; Jung, Jae-Pil; Kang, Choon-Sik; Shin, Yong-Eui
CS Department of Materials Science & Engineering, University of Seoul, Seoul, 130-743, S. Korea
SO Materials Transactions (2001), 42(5), 820-824
CODEN: MTARCE; ISSN: 1345-9678
PB Japan Institute of Metals
DT Journal
LA English
AB UBM-coated Si-wafer was fluxlessly soldered with glass substrate in N2 atmosphere using plasma cleaning method. The bulk **Sn**-37% **Pb** and **Sn**-3.5% Ag solders were rolled to the sheet of 100 .mu.m thickness to achieve bonding to Si-wafer by fluxless 1st reflow process. The oxide layer on the solder surface was analyzed by AES (Auger Electron Spectroscopy). After 1st reflow the Si-wafer with a solder disk was plasma-cleaned, and soldered to glass by 2nd reflow soldering process without flux in N2 atmosphere. The thickness of oxide layer decreased with increasing plasma power and cleaning time. The optimum plasma treatment condition in this study was 500 W for 12 min and at this condition, 100% bonding ratio for **Sn**-3.5 Ag and over 80% bonding ratio for **Sn**-37Pb solder were achieved. The intermetallic

compd. of continuous Cu6Sn5 was obsd. along the Si-wafer/solder interface but discrete Cu6Sn5 along the glass/solder interface and the different shapes of Cu6Sn5 were caused by different thickness of **Cu** as a pad. The fracture of the tensile test specimen occurred at not only solder/UBM and solder/TSM interface but also in Si-wafer and glass substrate.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 3 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:755488 HCAPLUS
DN 132:96449
TI Interfacial reactions of **tin**-zinc-bismuth alloys
AU Harris, Paul
CS ITRI Ltd, Uxbridge, UK
SO Soldering & Surface Mount Technology (1999), 11(3), 46-52
CODEN: SSMOEO; ISSN: 0954-0911
PB MCB University Press
DT Journal
LA English
AB A variety of **Pb**-free solders are now com. available. Of those suitable for **mass soldering** perhaps the ones closest to a direct, drop-in, replacement for **Sn**-**Pb** are the **Sn**-Zn-Bi alloys. For most **Sn**-based solders it is the **Sn** which is the active element and dominates the all-important interfacial reactions. As a result they have many properties in common. The addn. of Zn, however, radically alters this picture. Zinc oxidn. products are formed at the surfaces. Zinc intermetallic compds. are also formed in preference to **Sn**-compds. at the substrate interfaces. The nature and implications of these changes are outlined for 86Sn8.5Zn5.5Bi solders on the common base materials, 65Cu35Zn, **Cu**, Ni, and Ni42Fe58.

RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 4 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:300155 HCAPLUS
DN 130:345386
TI Phenomena in **soldered** joints with modest **solder masses**
AU Maiwald, W. J.
CS Germany
SO Int. Wiss. Kolloq. - Tech. Univ. Ilmenau (1998), 43rd(Band 2), 140-150
CODEN: IWKTEF; ISSN: 0943-7207
PB Technische Universitaet Ilmenau
DT Journal; General Review
LA German
AB A review with 6 refs. is given on phenomena appearing by reflow soldering in the surface mount technol. The reflow **soldering** (with modest **solder masses**) of ball grid array, chip size package, and flip chip devices showed several faults caused by chem. changes of the solder surface (incorporation of intermetallic phases). Furthermore, the influence of strong primary **Pb** crystn. was considered. Texture deviations in the soldered bumps due to the above mentioned reasons led to various kinds of damages. It was assumed that metallurgic processes in these cases no longer can be described using only binary system models (e.g. **Sn**-**Cu**, **Sn**-Au, **Sn**-Ni, **Sn**-Ag, **Sn**-Pd) but ternary and quaternary systems (e.g. **Sn**-**Cu**-Ni, **Sn**-**Cu**-Ni-Ag, **Cu**

-Ag-Au-Pd) have to be considered.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 5 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:266773 HCAPLUS
DN 128:311507
TI Brittle properties of **copper**-based **lead** frames at soldered joints
AU Haramaki, Takashi; Nakamura, Mitsuo; Mita, Mamoru
CS Hitachi, Ltd., Japan
SO Yosetsu Gakkai Ronbunshu (1998), 16(1), 105-109
CODEN: YGRODU; ISSN: 0288-4771
PB Yosetsu Gakkai
DT Journal
LA Japanese
AB **Copper** base alloys, contg. 2.4 mass% Fe and 0.1 **mass%** Zn, etc., were **soldered** using **Pb**-63 **mass%** **Sn** and then heated at 100.degree.C, 125.degree.C and 150.degree.C for 1000.apprx.2000 h to grow intermetallic compds. at the solder/alloy interface. Elemental anal. at the interface was performed by using EPMA. The fractured interface, where the solder was peeled off after the 30.degree. bending test, was obsd. by optical microscopy, and the concd. elements were analyzed by EPMA. The **copper** alloy contg. Fe, Zn showed a higher intermetallic compd. growth rate, thus larger decreasing in the peel strength at the soldered joint. Intermetallic compds. formed at the solder-**copper** alloy interface were found to be typically, at the solder side, .eta.-Cu6Sn5, and, at the **copper** alloy side, .epsilon.-Cu3Sn in which iron element was found to have been segregated.

L18 ANSWER 6 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:458392 HCAPLUS
DN 127:165549
TI Bonding of aluminum nitride to **copper** by surface modification. 2. Metalizing of AlN by ion plating
AU Saida, Kazuyoshi; Nishimoto, Kazutoshi; Fujimoto, Tetsuya; Tanaka, Katsuyuki; Fukaya, Yasuhiro
CS Fac. Eng., Osaka Univ., Japan
SO Yosetsu Gakkai Ronbunshu (1997), 15(2), 330-337
CODEN: YGRODU; ISSN: 0288-4771
PB Yosetsu Gakkai
DT Journal
LA Japanese
AB Metalization method of AlN substrate by ion plating technique has been developed. Dual coating films of 5-10 .mu.m thick nitrides (**TiN**, ZrN and CrN) and 10 .mu.m thick **copper** were formed on the AlN substrate by ion plating. The functionally gradient films of **TiN** .fwdarw. Ti were also deposited on the AlN substrate. The adherent strength of metalized films against AlN substrate was evaluated by the tensile test at room temp. The morphologies of nitride films were quite sound and they were stuck AlN together well. Element analyses by EPMA and ESCA revealed that nitrides such as **TiN**, ZrN and CrN were hardly reacted with AlN substrate of **Cu** film. The adherent strength of **TiN**, ZrN, CrN coating film and the functionally gradient films indicated the av. values of 50-60 MPa in any cases. The joint strength of **TiN+Cu** dual metalized AlN to **copper** **soldered** by **Sn**-38 **mass%Pb** **solder** was about 33 MPa.

L18 ANSWER 7 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:677521 HCAPLUS
DN 125:343930
TI Fluxless no-clean assembly of solder bumped flip chips
AU Koopman, N.; Nangalia, S.; Rogers, V.
CS MCNC, Research Triangle Park, NC, 27709, USA
SO Proc. - Electron. Compon. Technol. Conf., (1996), 46th, 552-558
CODEN: PETCES
DT Journal
LA English
AB MCNC has developed a radically new fluxless, no-clean process which has shown considerable success with assembly of a variety of flip chip configurations. The process, called PADS (Plasma Assisted Fluxless Soldering) relies on a pretreatment which enables the subsequent solder reflow in inert ambients. Conventional **mass** prodn. **soldering** tools can be used, just eliminating the flux dispense and flux cleaning steps, and adding the pretreatment step. Highlights of the applications studies will be presented. Examples will include high **lead** (97Pb3Sn) bumped flip chips joined to multilayer ceramic substrates with Mo/Ni/Au microsockets at 350.degree.C in nitrogen, eutectic **tin/lead** solder bumped flip chips joined at 250.degree.C to bare **copper**, 95/5 **lead/tin** bumped flip chips joined to eutectic dipped FR4 printed circuit boards, joining of 90/10 **lead tin** bumps to each other at 350.degree.C, unique MEMS (Micro Elec. Mech. Systems) devices joined with the dry fluxless process, and solder bumped flip chips joined to flexible circuits. Other related topics to be discussed include tacking, self alignment and its measurement, balling reflow, and rework operations including hot chip pull and site dress. Other areas of application of the fluxless process will be highlighted including hermetic seal band attachment, joining of flexible circuit TAB **leads** to insulator substrates, and joining to solid solder deposits on FR4.

L18 ANSWER 8 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:661641 HCAPLUS
DN 123:63149
TI Soldering of Ti + **Cu** dual metalized AlN to **copper** substrate - bonding of aluminum nitride to **copper** using surface modification technique (report 1)
AU Nakao, Yoshikuni; Nishimoto, Kazutoshi; Saida, Kazuyoshi; Fujimoto, Tetsuya; Murabe, Kaoru; Fukaya, Yasuhiro
CS Osaka Univ., Japan
SO Yosetsu Gakkai Ronbunshu (1995), 13(2), 240-7
CODEN: YGRODU; ISSN: 0288-4771
DT Journal
LA Japanese
AB Soldering of surface-modified AlN to **copper** was investigated using **Sn**-38 **mass%Pb solder**. AlN substrate was dually metalized by Ti and **Cu** using ion plating technique as follows: the 10 .mu.m thick Ti film was first plated on the AlN substrate, heat-treated in vacuum on various conditions and then the 5-10 .mu.m thick **Cu** film was plated on the heat-treated Ti film again. The thermal stress and heat condition analyses suggested that the soldered joints could possess the superior properties when the thickness of soldering layer was kept less than 0.4 mm. Defects such as microvoids and cracks were occurred in Ti film after heat treatment, and the fraction of defects increased with increasing the treating temp. and time. The tensile strength of Ti + **Cu** dual metalized AlN to **copper** joint was approx. 20 MPa, and slightly decreased as the treating time of

Ti film was increased. The Ti + **Cu** dual metalized AlN to **copper** soldered joint indicated the superior reliability for thermal fatigue and heat conduction.

L18 ANSWER 9 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:347621 HCAPLUS
DN 122:112927
TI Bonding of aluminum nitride to **copper** for reducing thermal stress
AU Nakao, Yoshikuni; Nishimoto, Kazutoshi; Saida, Kazuyoshi; Murabe, Kaoru; Fukaya, Yasuhiro
CS Faculty Engineering, Osaka University, Osaka, 565, Japan
SO Mater. Trans., JIM (1994), 35(12), 910-16
CODEN: MTJIEY; ISSN: 0916-1821
DT Journal
LA English
AB The crack susceptibility and properties of AlN to **copper** joints **brazed** with the Ag-27 **mass%Cu**-2%Ti filler metal and the **Sn**-38 **mass%Pb solder** were investigated. The heat conduction anal. suggested that the thermal conductivities of AlN-**copper** joints using the Ag-**Cu**-Ti insert metal added to tungsten interlayer and using the **Sn**-**Pb** solder with a thickness of less than 0.5 mm exceeded that of the AlN substrate (180 W/m.cntdot.K). Thermal stress distribution in the AlN-**copper** joints was numerically calcd. by a finite element method. The calcd. max. principal stress in AlN reduced by the use of a soft insert layer and/or a low expansivity interlayer. The crackings of brazed joints could be prevented when the tungsten interlayer thickness exceeded 0.8 mm in the brazed joint, and when the **Sn-Pb** solder was employed during the bonding operation. The tensile strength of the AlN-**copper** joints brazed at 1078 K for 120 s added to the 1.0 mm thick tungsten interlayer reached about 50 MPa, and that of the metalized AlN-**copper** soldered joints was about 20 MPa. The superior reliability for thermal cycling and heat conduction could be obtained for the AlN-W-**copper** joints using the Ag-**Cu**-Ti filler metal and titanium-**copper** multilayer-metalized AlN-**copper** joints using **Sn-Pb** solder.

L18 ANSWER 10 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1982:185707 HCAPLUS
DN 96:185707
TI Intermetallic compound growth and solderability
AU Davis, Paul E.; Warwick, Malcolm E.
CS Tin Res. Inst., Inc., Palo Alto, CA, 94306, USA
SO Plat. Electron. Ind. (1982), 9th, Paper No. 16, 19 pp.
CODEN: PELID5; ISSN: 0160-8576
DT Journal
LA English
AB The long-term storage of **Cu** components, coated with **Sn** or 60% **Sn**-40% **Pb** coatings and intended for use in elec. or electronic applications, permits the growth of intermetallic compd. layers (e.g., Cu3Sn) at the interface between the substrate surface and the protective solderable coating, even at ambient temps. This behavior results in a loss of solderability, particularly under **mass soldering** conditions since formation of the intermetallic layers reduces the thickness of the remaining, unreacted coating. Tests, using area of spread and surface tension balance methods, on artificially aged specimens and room temp. stds., indicate that solderability deteriorates significantly when the compd. thickness reaches

2-4 .mu.. Although the thickness of the remaining unreacted coating also has an effect on solderability parameters, this is less pronounced.

L18 ANSWER 11 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1975:502166 HCAPLUS
DN 83:102166
TI Effect of certain impurity elements on the wetting properties of 60% **tin**-40% **lead** solders
AU Ackroyd, M. L.; MacKay, C. A.; Thwaites, C. J.
CS Tin Res. Inst., Greenford/Middlesex, Engl.
SO Met. Technol. (London) (1975), 2, Pt. 2, 73-85
CODEN: MTNYAU
DT Journal
LA English
AB The effects of impurities on the wetting of **Sn**-40% **Pb** solder on **Cu**, brass, and mild steel were studied. Solderability was evaluated by spreading-area and rotary-dip tests. The lowest impurity levels producing oxidn. and/or wetting redn. were Al 0.0005, Sb 1.0, As 0.005-0.2, Bi 0.5, Cd 0.15, **Cu** 0.29, P 0.01, S 0.0015, and Zn 0.003%. These levels differ somewhat from national specification limits and are of importance in **mass-soldering** applications.

L18 ANSWER 12 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1965:437706 HCAPLUS
DN 63:37706
OREF 63:6690f-g
TI Removing adherent solder from metallic and other articles
IN Lantz, Lloyd C.
SO 3 pp.
DT Patent
LA Unavailable
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 3187423		19650608	US	19620104

AB Solder spattered or remaining in excess in undesired locations near soldered joints or on such delicate equipment as printed circuit boards is more easily removed after alloying with an approx. equal amt. of a Hg alloy contg. .apprx.23% each of **Pb** and **Sn** by wt. This alloy is soft and can be easily cut at room temp. When melted at .apprx.110.degree.F. with a hot tool on a spilled **solder mass**, the Hg alloy mixes with the solder, converting it to a Hg alloy that adheres much less readily to any base, and remains in the pasty nonadherent state for a longer period while cooling. If too much Hg is added, the alloy stains **Cu** which it contacts, and the stain is difficult to remove. Flux can be used with the alloy for rapid heating, but is not required. The alloy is easily made from the 3 metals at 450.degree.F. Soldered joints from which solder is removed in this way are readily resoldered after brushing.

L20 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:674337 HCAPLUS
TI Microelectronic packages with solder interconnections
IN Distefano, Thomas H.
PA Distefano, Thomas, USA
SO U.S. Pat. Appl. Publ., Division of Ser. No. US 1998-157047, filed on 18 Sep 1998 which
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001020748	A1	20010913	US 2001-854269	20010511
	US 6335222	B1	20020101	US 1998-157047	19980918
PRAI	US 1997-59225P	P	19970918		
	US 1998-157047	A3	19980918		

AB A soldered assembly for a microelectronic element includes a microelectronic element, **solder columns** extending from a surface of the microelectronic element and terminals connected to **distal** ends of the columns. The assembly can be handled and mounted using conventional surface-mount techniques, but provides thermal fatigue resistance. The **solder columns** may be inclined relative to the chip surface, and may contain long, columnar inclusions preferentially oriented along the lengthwise axes of the columns.

L23 ANSWER 1 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:516235 HCAPLUS
TI Edge clip **terminal**
IN Dennis, Richard K.
PA Die Tech, Inc., USA
SO U.S., 10 pp., Cont.-in-part of Ser. No. US 1999-302691, filed on 30 Apr 1999
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6261136	B1	20010717	US 2000-613260	20000710
US 1999-302691	A2	19990430		

AB A double sided edge clip **terminal** for forming soldered connections with opposed contact pads on the edge of a substrate includes a pair of solder contacts each having spaced metal arms and cold extruded **solder masses** in the interior of the contacts between the arms. Openings are formed in the contacts between the arms to prevent wicking of molten solder along the **terminal** and away from the contact pads. The **terminals** are manufactured by extruding the **solder masses** through the openings and into the space between the arms and beyond the arms, without solder waste.
RE.CNT 27 THERE ARE 27 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 2 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:784546 HCAPLUS
TI Edge clip **terminal** and method
IN Dennis, Richard K.
PA Die Tech, Inc., USA
SO PCT Int. Appl.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2000067346	A1	20001109	WO 2000-US10315	20000417

PI
W: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

PRAI US 1999-302691 A 19990430
AB A double sided edge clip **terminal** (16) for forming soldered connections with opposed contact pads (66) on the edge of a substrate (64) includes a pair of solder contacts (20, 22) each having spaced metal arms (40) and cold extruded **solder masses** (32, 34) in the interior of the contacts between the arms. Openings (42) are formed in the contacts between the arms to prevent wicking of molten solder along the **terminal** and away from the contact pads. The

terminals are manufactured by extruding the **solder masses** through the openings and into the space between the arms and beyond the arms, without solder waste.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:410755 HCAPLUS
DN 103:10755
TI Oxygen sensor with heater
IN Kato, Nobuhide; Murase, Takao
PA NGK Insulators, Ltd., Japan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4512871	A	19850423	US 1984-604473	19840427
	US 4528086	A	19850709	US 1984-604474	19840427
PRAI	JP 1983-U68663		19830509		
	JP 1983-U68664		19830509		
	JP 1983-U202830		19831223		
	JP 1983-U202831		19831223		
	JP 1983-68665		19830509		

AB An O sensor for detecting O in exhaust gase from an internal combustion engine comprises a tubular solid electrolyte body having an elongate bore closed at one end and having porous Pt electrodes on its inner and outer surfaces; a housing supporting the solid electrolyte such that its outer surface is exposed at the closed end to exhaust gas and such that the elongate bore is gas-tight to the exhaust gas; and a bar-shaped heater inserted into the elongate bore in the tubular solid electrolyte body. The bar-shaped heater comprises a heating resistor having a pos. temp. coeff., a ceramic body having a pair of **terminal** pads connected to the heating resistor, and a pair of lead wires brazed to the pads with a **mass** of **brazing** material contg. Ag. An exposed surface of the **brazing mass** is coated with a metal layer, e.g., Ni, which can be further coated with a heat-resistant layer.

L23 ANSWER 4 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 1981:614007 HCAPLUS
DN 95:214007
TI Recent developments on condensation soldering external leads to hybrid integrated circuits
AU Gutbier, E. A.; Chavers, R. A.; Ouellette, P. J.
CS Western Electr. Co. Inc., North Andover, MA, 01845, USA
SO Proc. - Electron. Compon. Conf. (1981), 31st, 181-6
CODEN: PECCA7; ISSN: 0569-5503
DT Journal
LA English
AB From visual observations in a transparent lab. condensation soldering facility, upon melting of the **solder** preform, nearly the entire **mass** of the molten metal flowed upward along the main **terminal** surfaces and, after reaching equil., the molten mass reversed its directional motion, flowing downward, completing the solder bonds. Occasionally, this solder flow behavior has led to the formation of questionable solder connections. In light of these observations, **terminal** design changes were introduced to preserve lead

solderability and to more effectively control solder flow dynamics necessary for improving bond yields. By changing the Sn-Pb **terminal** finish to pure Sn (applied either by reflowing a Sn electrodeposit or by a hot Sn coating), the m.p. was now increased nearly 20.degree. above the b.p. of the primary working fluid (i.e., 215.degree.). Consequently, the new Sn finish did not melt and thus retained its original thickness. By introducing further **terminal** modifications, the sequential solder flow pattern was significantly altered. The molten solder was forced to flow downwardly onto the circuit path immediately upon melting of the solder preform. Finally, metallog. cross sections, high-speed photographs, and other anal. results are shown which aided in the investigation and formed the basis for the conclusions.

L29 ANSWER 1 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:753381 HCAPLUS
TI Thin, stackable semiconductor packages
IN Lee, Seon Goo
PA Anam Semiconductor, Inc., S. Korea; Amkor Technology, Inc.
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6303997	B1	20011016	US 1999-287711	19990407
JP 3196026	B2	20010806	JP 1999-68670	19990315
PRAI KR 1998-12364	A	19980408		

AB A thin, stackable semiconductor package having improved electrical and heat dissipating performance comprises a semiconductor **chip** having an **integrated circuit** and a plurality of input/output pads on a surface thereof. A lead frame having a plurality of inner leads with upper and a lower surfaces has one of those surfaces bonded to a surface of the **chip** with a bonding agent. The leads each has a projection formed on at least one of the upper and lower surfaces at a **distal** end portion of the lead. Each of the leads is electrically connected to an associated input/output pad of the **chip** through a wire bonding process using electrically conductive wires, or by a ball bonding process using electrically conductive balls. Alternatively, the leads may be directly bonded to the input/output pads of the **chip** by a TAB bonding process. An encapsulated portion envelops the semiconductor **chip** and the leads while exposing the projections of the leads to the atmosphere outside the encapsulated portion. A solder ball is welded to the bottom surface of the projection of each lead and is used as a signal input/output **terminal** of the package. A **chip** heat sink may be bonded to the **chip** to further increase the capacity of the package to dissipate heat away from the **chip** during operation.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 2 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:710799 HCAPLUS
TI Contact sheet
IN Ochiai, Toshimasa
PA Ngk Insulators, Ltd., Japan
SO U.S. Pat. Appl. Publ., Cont.-in-part of Ser. No. US 1999-410377, filed on 30 Sep 1999
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2001024892	A1	20010927	US 2001-730229	20010416
PRAI US 1999-410377	A2	19990930		

AB A contact sheet used with a socket for connecting an **integrated circuit** having spherical **terminals** to a board includes: protruding contact springs in some or all of numerous through holes provided in a sheet composed of an insulative elastic material, wherein each of the contact springs is composed of a conductive material and

L29 ANSWER 3 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:674337 HCAPLUS
TI **Microelectronic** packages with solder interconnections
IN Distefano, Thomas H.
PA Distefano, Thomas, USA
SO U.S. Pat. Appl. Publ., Division of Ser. No. US 1998-157047, filed on 18 Sep 1998 which
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2001020748	A1	20010913	US 2001-854269	20010511
US 6335222	B1	20020101	US 1998-157047	19980918
PRAI US 1997-59225P	P	19970918		
US 1998-157047	A3	19980918		

AB A soldered assembly for a **microelectronic** element includes a **microelectronic** element, solder columns extending from a surface of the **microelectronic** element and **terminals** connected to **distal** ends of the columns. The assembly can be handled and mounted using conventional surface-mount techniques, but provides thermal fatigue resistance. The solder columns may be inclined relative to the **chip** surface, and may contain long, columnar inclusions preferentially oriented along the lengthwise axes of the columns.

L29 ANSWER 6 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:666146 HCAPLUS
TI Reflective liquid crystal display and connection assembly and method
IN Takiar, Hem P.; Mathew, Ranjan J.
PA National Semiconductor Corporation, USA
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5969783	A	19991019	US 1998-209868	19981211

AB A connection assembly (40) for operably coupling a plurality of independent imaging devices (41, 41;, 41") to an optical subsystem (42). The connection assembly (40) includes a unitary flex circuit device (43) having an elongated arm portion (45), and a plurality independent finger portions (46, 46', 46") extending from a **distal** end of the arm portion (45). Each finger portion (46, 46', 46") defines a coupling region (47, 47', 47") adapted to operably couple a respective imaging device (41, 41', 41") to a respective finger portion (46, 46', 46") for support thereof. The finger portions (46, 46', 46") are further adapted to strategically couple each respective imaging device (41, 41', 41") to the optical subsystem (42) as a unit. The flex circuit device (30) includes a plurality of circuits (65) terminating at respective **terminals** (40) of a coupling region (47) thereof. The **terminals** (66) supportively and communicably coupled to the bond pads (67) of the **die** (58) for support thereof. The coupling region (47) further includes an adhesive mount (76) mounting the flex circuit device (43) to the transparent plate to supportably suspend the display assembly (57) between the **die** (58) and the transparent plate (61).

L29 ANSWER 12 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1972:65375 HCAPLUS
DN 76:65375
TI Semiconductor devices with rectifying junctions
IN Eriksson, Lars O.
PA General Electric Co.
SO Brit., 6 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI GB 1258309		19711230		
PRAI US		19680409		

AB A semiconductor device is provided in which a semiconductor body, having .gtoreq.1 rectifying junction, is elec. interposed between a pair of electrodes. A high-current semiconductor rectifier, e.g., includes a disk-like body sandwiched between the flat bottoms of a pair of cup-shaped **terminal** members whose rims are bonded to opposite ends of a hollow elec. insulator to form an integral, hermetically sealed housing for the body. The cup-shaped **terminal** members extend axially inward, enabling the body to be mounted under pressure between the opposing ends of a pair of force-transmitting elec. conductive thrust members that are received in the cup-shaped **terminals** and serve as combined elec. and thermal conductors. The disk-like body is a thin, broad-area, circular **wafer** of asym. conductive Si on a thicker substrate of W or Mo with a facing of Au-Ni on the **distal** end of the substrate and a thin metal contact overlying the top surface of the Si. The contact is preferably Au, but other metals can be used. The anode is joined to the insulator by means of a sidewall integrally connected to the flared rim, which in turn is attached to a metallized lower end of the insulator. A similar **terminal** member is formed by the cathode except that the sidewall is noncircular to allow a lead connection to a ring gate. The thrust members are cylindrical and made of

L36 ANSWER 1 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:924240 HCAPLUS
DN 136:46915
TI Design and fabrication of a semiconductor device having conventional gull-wing and straight outer leads
IN Sugihara, Koichi; Miyashita, Koichi
PA Japan
SO U.S. Pat. Appl. Publ., 18 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001052643	A1	20011220	US 1999-324774	19990603
PRAI JP 1998-155950	A	19980604		

AB A conventional semiconductor device having conventional gull-wing and straight outer leads and a manufg. method of such a semiconductor device are described. Outer leads extend outward from within a **package** that seals a semiconductor **chip**, and they are **connected** to the semiconductor **chip** inside the **package**. Depressions are formed at the **distal** end portions of the outer leads. The depressions are coated with a material which is one of the following: Sn-Pb, Sn-Ag, Sn-Bi, Sn-Zn, Sn-Cu, Pd, Au, and Ag. The depressions are V-shaped, U-shaped, or rectangular. Each depression has a depth which is 30% to 75% with respect to the thickness which the outer lead has at the cut end face of **distal** end thereof. The outer leads are either a gull-wing type or a straight type.

L36 ANSWER 2 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:653929 HCAPLUS
TI Raised pedestal radiation shield for sensitive electronics
IN Benedetto, Joseph M.
PA Utmc Microelectronic Systems Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6121672	A	20000919	US 1998-185162	19981103

AB A radiation shield for **protecting** an **integrated circuit** device from harmful radiation has a high Z shielding material for absorbing radiation. The radiation shield has a planar lower surface in contact with an upper surface of the **integrated circuit** device. The radiation shield also has a central portion in substantial registration with **integrated circuit** device. The central portion has a thickness sufficient to absorb harmful radiation. A **distal** portion is located about the central portion. A transitional portion is located between and **connects** the central and **distal** portions. The transitional portion has a minimum thickness, as, measured from the **integrated circuit**, that is about equal to the thickness of the central portion.
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:672231 HCAPLUS
DN 135:219607
TI Metal contact module for a smart card, credit card, or identification card and method for making same
IN Chung, Kevin Kwong-tai
PA Amerasia International Technology Inc., USA
SO U.S., 20 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6288905	B1	20010911	US 1999-412052	19991004
EP 1138181	A1	20011004	EP 1999-953156	19991014
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				
PRAI US 1998-104337P	P	19981015		
US 1999-129497P	P	19990415		
US 1999-131377P	P	19990428		
US 1999-134656P	P	19990518		
US 1999-141344P	P	19990628		
WO 1999-US23850	W	19991014		

AB A module, such as a contact module for embedding an electronic device into a credit card, smart card, identification tag or other article, comprise a pattern of metal contacts having a 1st and a 2nd surface and elec.-conductive vias built up on the 1st surface of the metal contacts. A layer of **dielec**. adhesive on the 1st surface of the pattern of metal contacts surrounds the elec.-conductive vias except the ends thereof **distal** from the metal contacts. An electronic device has elec. contacts **connected** to the exposed ends of the conductive vias, as by wire bonds or by flip-**chip** type **connections**. The module is preferably made by forming a pattern of conductive vias on the 1st surface of a sheet of elec. contact material, the pattern of vias corresponding to the pattern of contacts of an electronic device; applying **dielec**. adhesive on the 1st surface of the sheet of elec. material except in locations corresponding to the vias; patterning the sheet of elec. material to define a pattern of elec. contacts thereon, wherein ones of the elec. contacts are assocd. with at least corresponding ones of the vias; and attaching the electronic device with the contacts of the electronic device elec. **connected** to corresponding vias.
RE.CNT 37 THERE ARE 37 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:25976 HCAPLUS
TI Arc resistant high voltage micromachined electrostatic switch
IN Goodwin-Johansson, Scott Halden
PA Mcnc, USA
SO PCT Int. Appl.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI WO 2001003152 A1 20010111 WO 2000-US12142 20000504
W: AE, AG, AL, AM, AT, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, CZ, DE, DE, DK, DK, DM, DZ, EE, EE, ES, FI, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG
EP 1196932 A1 20020417 EP 2000-930355 20000504
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO
PRAI US 1999-345300 A 19990630
WO 2000-US12142 W 20000504

AB A MEMS (Micro Electro Mech. System) electrostatically operated device is provided that can switch high voltages whiles providing improved arcing tolerance. The MEMS device comprises a **microelectronic** substrate, a substrate electrode, first and second contact sets, an **insulator**, and a moveable composite. The moveable composite overlies the substrate and substrate electrode. In cross section, the moveable composite comprises an electrode layer and a biasing layer. In length, the moveable composite comprises a fixed portion attached to the underlying substrate, a medial portion, and a **distal** portion moveable with respect to the substrate electrode. Each contact set has at least one composite contact attached to the moveable composite, and preferably at least one substrate contact attached to the substrate. One of the contact sets is closer to the composite **distal** portion. The **distal** and/or medial portions of the moveable composite are biased in position when no electrostatic force is applied. Applying a voltage between the substrate electrode and moveable composite electrode creates an electrostatic force that attracts the moveable composite to the underlying substrate. The first and second contact sets are elec. **connected** when the **distal** portion of the moveable composite is attracted to the substrate. Once electrostatic force is removed, the moveable composite reassumes the biased position such that the first and second contact sets are disconnected in a sequence to minimize arcing. Various embodiments and methods of using the electrostatic MEMS device are provided.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:23050 HCAPLUS
TI Gas injection system for plasma processing
IN Mcmillin, Brian; Nguyen, Huong; Barnes, Michael; Ni, Tom
PA Lam Research Corporation, USA
SO U.S., Cont.-in-part of Ser. No. US 1996-672315, filed on 28 Jun 1996
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 3

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6013155	A	20000111	US 1997-885353	19970630
WO 9900532	A1	19990107	WO 1998-US13777	19980630

W: JP, KP
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE

	EP 1017876	A1	20000712	EP 1998-931773	19980630
	R: AT, DE, FR, GB, IT, NL, IE				
	JP 2002511905	T2	20020416	JP 1999-505915	19980630
	KR 2000022193	A	20000425	KR 1998-710611	19981224
	US 6270862	B1	20010807	US 1999-359639	19990726
PRAI	US 1996-672315	A2	19960628		
	US 1997-885353	A	19970630		
	WO 1998-US13777	W	19980630		

AB A plasma processing system for plasma processing of substrates such as semiconductor **wafers**. The system includes a plasma processing chamber, a substrate support for supporting a substrate within the processing chamber, a **dielectric** member having an interior surface facing the substrate support, the **dielectric** member forming a wall of the processing chamber, a gas supply comprising one or more injector tubes extending rectilinearly in the plasma processing chamber and having one or more orifices in a sidewall for supplying gas into the chamber, and an RF energy source such as a planar coil which inductively **couples** RF energy through the **dielectric** member and into the chamber to energize the process gas into a plasma state. The gas is supplied through orifices located outside of regions at the **distal** tip of the injector tubes where electric field lines are concentrated. The arrangement minimizes clogging of the orifices since the orifices are located away from areas where most build-up of process byproducts occur on the injector tube.

RE.CNT 24 THERE ARE 24 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L39 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:666177 HCAPLUS
TI Semiconductor fabrication employing a local interconnect
IN Gardner, Mark I.; Kadosh, Daniel; Spikes, Jr Thomas E.
PA Advanced Micro Devices, Inc., USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5970375	A	19991019	US 1997-851086	19970503

AB An **integrated circuit** fabrication process is provided in which a sub-level local interconnect is formed between a gate conductor of one transistor and a junction of another transistor. The formation of a sub-level local interconnect allows for higher packing density by removing the local interconnect to a sub-level **dielectrically** spaced from possibly other local interconnects and from the **distal** interconnect normally associated with device interconnection. A semiconductor topography is provided which includes a first transistor laterally spaced from a second transistor, the transistors being arranged upon and within the substrate. An interlevel **dielectric** is deposited across the semiconductor topography. A portion of the interlevel **dielectric** is removed to form a trench. The trench is then filled with a conductive material to form a local interconnect extending horizontally above a portion of the first transistor and a portion of the second transistor. Portions of the interlevel **dielectric** and the local interconnect are removed in sequence while retaining the patterned masking layer. Removal of the local interconnect forms vias extending to the gate conductor of one transistor and to a junction of the other transistor, or from the gate conductor of

one transistor to a junction of the same transistor. A conductive material may be deposited in these vias to form plugs therein. Further, a capping **dielectric** layer may be deposited upon the interlevel **dielectric** and contact regions may be formed which abut the plugs. Therefore, **distal** interconnect conductive layers may then be formed **dielectrically** above the local interconnect which are then electrically **coupled** to the local interconnect through the contact regions.

L39 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:35025 HCAPLUS
DN 130:89427
TI Gas injection system for plasma processing apparatus for semiconductor substrates
IN Mcmillin, Brian; Nguyen, Huong; Barnes, Michael; Ni, Tom
PA Lam Research Corporation, USA
SO PCT Int. Appl., 50 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9900532	A1	19990107	WO 1998-US13777	19980630
	W: JP, KP				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 6013155	A	20000111	US 1997-885353	19970630
	EP 1017876	A1	20000712	EP 1998-931773	19980630
	R: AT, DE, FR, GB, IT, NL, IE				
	JP 2002511905	T2	20020416	JP 1999-505915	19980630
PRAI	US 1997-885353	A	19970630		
	US 1996-672315	A2	19960628		
	WO 1998-US13777	W	19980630		

AB A plasma processing system for plasma processing of substrates such as semiconductor **wafers** is claimed. The system includes a plasma processing chamber, a substrate support within the processing chamber, a **dielec**. member having an interior surface facing the substrate support forming a wall of the processing chamber, and a gas supply comprising one or more injector tubes extending rectilinearly in the plasma processing chamber and having one or more orifices in a sidewall for supplying gas into the chamber. Finally it has an RF energy source such as a planar coil which inductively **couples** RF energy through the **dielec**. member and into the chamber to energize the process gas into a plasma state. The gas is supplied through orifices located outside of regions at the **distal** tip of the injector tubes where elec. field lines are concd. The arrangement minimizes clogging of the orifices since the orifices are located away from areas where most build-up of process by products occur on the injector tube.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L43 ANSWER 9 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1987:469129 HCAPLUS
DN 107:69129
TI Multilayer circuit boards
IN Tanaka, Minoru; Shoji, Fusaji; Yokono, Ataru; Murata, Akira; Hirota, Kazuo
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 61212096	A2	19860920	JP 1985-52270	19850318
	JP 05082972	A2	19930402	JP 1992-61753	19920318
PRAI	JP 1985-52270		19850318		

AB A multilayer circuit board has, at least on one side, alternate insulator and conductor interconnection layers, in which the conductor layers are elec. **connected** via a conductor in through holes. The board consists of an alloy substrate **contg**. Ni 30-50, Co 0-5 wt.%, and Fe balance. The insulator is a polyimide with a thermal-expansion coeff. .ltoreq.4 x 10-5 degree-1. Optionally, the polyimide film may be adhered to the substrate or the conductor interconnection layer with a polyimide adhesive with a similar thermal-expansion coeff. The board is useful for **integrated circuits** having a no. of **logic circuits**.

L43 ANSWER 10 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:79976 HCAPLUS
DN 102:79976
TI Hardening of precursors for heat-resistant polymers
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 59184226	A2	19841019	JP 1983-58784	19830405

AB Precursors are exposed to microwave radiation to prep. heat-resistant polymers such as org. heterocyclic polymers and ladder silicones. Thus, a varnish (15% solids) **contg**. a 4,4'-diaminodiphenyl ether-pyromellitic dianhydride copolymer [**25038-81-7**] precursor was coated on a Si **wafer**, dried, and irradiated with microwave to form a **uniform insulating** coating having flexibility and heat resistance temp. 460.degree..

L43 ANSWER 11 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1983:82420 HCAPLUS
DN 98:82420
TI Interconnection-structure **body**
PA Hitachi, Ltd., Japan
SO Jpn. Tokkyo Koho, 6 pp.
CODEN: JAXXAD
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 57036759	B4	19820805	JP 1974-129969	19741113

AB In an interconnection-structure **body** consisting of a circuit board, polyimide or PIQ insulator film on the circuit board, and interconnection layer over the circuit board and/or insulator film, a thin film of a heat-treated Al chelate compd. is provided between the circuit board and insulator film to improve the adhesion strength. The interconnection-structure **body** is useful for a hybrid **integrated circuit**

L46 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:619387 HCAPLUS
DN 127:294297
TI Flip **chip** bonding of semiconductor elements
IN Ozawa, Takashi
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09246326	A2	19970919	JP 1996-53329	19960311

AB The process for flip **chip** bonding of .gtoreq.2 semiconductor elements on which **bumps** are formed, onto electrodes formed on bonding substrates, consists of adhering resins onto the tops of the **bumps**, adhering microcapsules consisting of cond. fillers coated with elec. insulators onto the resins, and hot press bonding the semiconductor elements on the electrodes. The process may be repeated for each semiconductor element. Alternatively, resins **contg**. the microcapsules are adhered onto the tops of the **bumps**. The **bumps** may be stud **bumps**. The process provides high-d. packaging.